I CLAIM AS MY INVENTION:

1. An arrangement for printing a print image with regions of said print image having respectively different print image resolutions comprising:

a printhead adapted to print a print image on an item moving past said printhead;

an encoder that generates signals indicative of movement of said item relative to said printhead;

a pixel memory;

a microprocessor connected to said pixel memory, said microprocessor causing pixel data to be stored in said pixel memory in compressed form in a plurality of data strings each containing a plurality of data words;

a print data controller connected to said encoder, said microprocessor, said pixel memory, and said printhead for controlling transfer of said pixel data word-by-word from said pixel memory to one of two buffer memories of said print data controller for intermediate storage therein in the form of a data string having a switchable number of data words with pixel data in compressed form and dependent on the required resolution for a region of said print image, for editing the data words stored in the other of the buffer memories and supplying the pixel data to said printhead, wherein said print data controller is equipped to supplement pixel data missing because of the comparison dependent on the required resolution for a region of said print image and for printing said image column-by-column with said printhead said print data controller having two buffer memories; and

said microprocessor, for a selected region of said image, setting a print image resolution for said region and is programmed to supply at least one parameter for the control of the resolution to the print data controller and the print data controller correspondingly switches the resolution that will be achieved in printing.

2. An arrangement as claimed in claim 1 wherein the microprocessor is programmed to communicate a start value for high resolution to the printer controller via bus, that the print data controller is composed of a pixel data editing unit, a DMA controller, an address generator and a printer controller, whereby the printer controller is connected in terms of control to the DMA controller, to the address generator and to the pixel data editing unit.

3. An arrangement as claimed in claim 1 wherein the printer controller is equipped with means for generating an F_A-signal and an F_D-signal corresponding to the factors, for controlling the printing with different resolution whereby the factors are equal to the value "one" of the start value (HRS) or different from the value "zero" of the start value, whereby the factors are set at least equal to the value "two", whereby the DMA controller can be switched by an FD signal communicated via a control line, such that the plurality of DMA cycles is at least halved when loading binary pixel data into a buffer memory of the pixel data editing unit, and whereby the address generator is switchable by an FA signal communicated via a control line such that at least halved read addresses for a read access onto the buffer memories of the pixel data editing unit are then generated.

4. An arrangement as claimed in claim 3 wherein the ratio of the maximum plurality of DMA cycles to the reduced plurality of DMA cycles corresponds to the compression factor communicated via FD signal, and that the compression factor applied to one and the same data string is equal to the decompression factor communicated via FA signal.

5. An arrangement as claimed in claim 1 wherein the pixel data editing unit contains a selector and a shift register, whereby the selector is connected to the buffer memories for the selection of the binary pixel data and is equipped with the means for supplementing the pixel data missing due to the compression, and whereby the shift register is connected to the output of the selector for parallel/serial conversion and offers the binary pixel data in a sequence required for the type of printhead.

6. An arrangement as claimed in claim 1 wherein the printer controller is connected in terms of control to the DMA controller, the address generator and the pixel data editing unit: wherein a DMA start signal is communicated to the DMA controller that, as a result of a plurality of implemented DMA cycles, makes the pixel data of a data string available by data strings to the pixel data editing unit; wherein an AG start signal is communicated from the printer controller to the address generator, whereby the address generator comprises a unit for generating read addresses and an address read signal former dependent on the decompression factor, whereby the address read signal corresponds to the quotient of the read addresses generated for a read access onto the buffer memories and the decompression factor; and wherein the pixel data editing unit comprises a first buffer memory and a second buffer memory for each printhead, whereby the buffer

memories store a data string in alternation and comprise an address input for applying the address read signal.

7. An arrangement as claimed in claim 6 wherein the printer controller is fashioned with means for generating a switchover signal and is connected to the DMA controller as well as to the pixel data editing unit, whereby the switchover signal comprises a first value "one" for preventing the readout from the respectively first buffer memory and for allowing the readout from the respectively second buffer memory or, respectively, whereby the switchover signal comprises a second value "zero" for allowing the readout from the respectively first buffer memory and for preventing the readout from the respectively second buffer memory.

8. An arrangement as claimed in claim 6 wherein at least the less-significant addresses of the address read signal also is present at the selector of the pixel data editing unit, and that the address generator comprises a primitive address signal generator and a write signal generator connected to said selector.

9. An arrangement as claimed in claim 6 wherein the first and second buffer memories are each a dual-port RAM; and wherein the selector comprises a first multiplexer that selects a single bit of the binary pixel data when the less significant part of the address read signal is present at its address input, whereby the first multiplexer following the first dual-port RAM has an output side connected to a first data input of a third multiplexer, and whereby a second multiplexer following the second dual-port RAM has an output side connected to a second data input of the third multiplexer; wherein a switchover signal is present at the control input of the third multiplexer, so that said single bit of the binary pixel data is output and is present at the data input of a following, fourth multiplexer and is through-connected to the data input of a following demultiplexer when an additional address signal

having a first value "one" is present at the control input; wherein the demultiplexer is followed by a resettable collecting register for binary pixel data that comprises a 14-bit parallel data output, whereby said single bit of the binary pixel data is transferred into the collecting register when a write signal is applied to a control input of the collecting register; in that the primitive address signal that sets the memory location of the bit in the collecting register is supplied to the demultiplexer.

10. An arrangement as claimed in claim 9 wherein the address generator comprises an input/output logic and a selection logic that is circuited between the unit for generating read addresses and the address read signal former; in that the selection logic is operated for the selection of read addresses dependent on the decompression factor.

11. An arrangement as claimed in claim 10 wherein the output of the third multiplexer is directly connected to the data input of the following demultiplexer; and wherein an additional voltage potential having the value "zero" is present at respective further data inputs of said first and second multiplexers, said additional voltage potential having the value "zero" being through-connected onto the output of the first and second multiplexers, whereby the additional address signal is generated by the selection logic as a component of the address read signal.

12. An arrangement as claimed in claim 11 wherein the selection logic generates the additional address signal that is applied to the selector; in that a voltage potential having the value "zero" is present at the other input of the fourth multiplexer for supplementing the value of the pixel data missing due to the compression, whereby a switch is made onto the voltage potential having the value "zero" when the additional address signal comprises the value "zero".

13. An arrangement as claimed in claim 11 wherein the unit for generating read addresses comprises a first counter for the primitive address and an allocated, first comparator for the comparison of a count value of the primitive address to a first rated value that is supplied from a register, and comprises a second counter for an address group and an allocated, second comparator for the comparison of a count value of the address group to a second rated value that is supplied from a register, and also comprises an executive sequencer, whereby the comparison in the first comparator is undertaken after a formation of the address read signal and after an incrementation of a count value for the primitive address by the value "one", whereby the counter for an address group is incremented by the value "one" after a plurality of read addresses are successively generated, an upward transgression of a rated value or, respectively, an overflow of the counter for the primitive address is triggered, a load signal is output and a sub-routine for the output is started, whereby a downward transgression of the second rated value in the comparison in the second comparator triggers a resetting of the count value of the primitive address to the value "one" and a generation of a following read address that belongs to a further address group.

14. An arrangement as claimed in claim 10 wherein the input/output logic of the address generator comprises an input for the communicated decompression factor, an input for receiving a start value for a variable, a register for the additional address signal, an input for the reception of the address generator start signal and a register for the address generator busy signal to be sent; in that the selection logic comprises a register for the variable and a first comparison logic for generating the additional address signal with the value "zero" that is generated when both the variable and the decompression factor communicated from the printer controller in

the FA-signal are set to a value unequal to "one" or when the decompression factor is set to a value unequal to the value "one" and the variable is equal to the value "one" and the decompression factor is set to a value unequal to the value "two" and the count value of the address group is an even number.

15. An arrangement as claimed in claim 14 wherein the selection logic comprises a second comparison logic for generating the additional address signal with the value "one" that is generated when the decompression factor communicated from the printer controller in the FA-signal is set to the value "one".

16. An arrangement as claimed in claim 15 wherein a further comparator in addition to the second comparison logic are arranged for generating the additional address signal with the value "one" that is generated when the decompression factor is set to a value unequal to the value "one" and the variable is equal to the value "one" and the decompression factor is set to a value equal to the value "two" or the decompression factor is set to a value unequal to the value "two" and the count value of the address group is not an even number.

17. An arrangement as claimed in claim 14 wherein the value of the register for the variable is set to the value "one" when the selection logic generates the additional address signal with the value "zero"; and in that the selection logic resets the value in the register for the variable to the value "zero" with every generation of the additional address signal with the value "one".

18. An arrangement as claimed in claim 14 wherein a comparator is provided in the selection logic so that the address read signal is generated only from read addresses having a positive value.

19. An arrangement as claimed in claim 10 wherein the address read signal former includes a shift register in which a binary number stored corresponding

to the generated read address is shifted by at least one place when a decompression factor that deviates from the value "one" is present in an input of the address generator.

20. An arrangement as claimed in claim 10 wherein the die unit for generating a read address comprises a plurality of counters that are connected in terms of circuitry in order to couple the formation of the address read signal to a primitive address signal such that every count value for the primitive address repeats and a plurality of read addresses can be allocated to each count value, whereby at least one group of read addresses is selected by the selection logic dependent on the variable and on the decompression factor.

21. An arrangement as claimed in claim 20 wherein the executive sequencer is connected to a signal generator for generating a write signal, to a signal generator for generating a load signal, to a signal generator for generating a print start signal and to an AG-busy signal generator; as well as in that the input/output logic of the address generator comprises a register for the output of the primitive address, a register for the write signal, a register for the load signal, a register for the output of the address read signal and a register for the output of the print start signal.

22. An arrangement as claimed in claim 6 wherein the printer controller comprises a data string counter and is connected to the encoder, whereby the value of the data string counter is incremented after every printed data string given the appearance of the encoder clock, whereby the value of the high resolution signal is changed when a prescribed, first rated value of the data string counter is reached, and whereby the printing of the print image is ended when a prescribed, second rated value of the data string counter is reached.

23. An arrangement as claimed in claim 1 wherein the further rated value registers and comparators are present in order to modify the current print resolution with every further equality of the rated value of one of the rated value registers with the current count value of the data string counter.

24. An arrangement as claimed in claim 1 wherein the printer controller comprises a first switchover in order to change the compression factor to the value equal to "one" when the high resolution signal has the value "zero" and is switched to the value equal to "one"; and in that the printer controller comprises a second switchover in order to change the compression factor to a predetermined, even-numbered value when the high resolution signal has the value equal to "one" and is switched to the value equal to "zero".

25. An arrangement as claimed in claim 24 wherein the printer controller comprises a logic to match the decompression factor to the current compression factor when the DMA controller and the address generator output a busy signal with the value "zero".

26. An arrangement as claimed in claim 24 comprising further reference value registers and comparators for modifying a current print resolution upon each equality of a value of "one" of the reference value registers with the current count value of the data string counter.

27. An arrangement as claimed in claim 1 wherein a further switchover logic or is arranged in the printer controller or in the address generator, said further switchover logic or changing a start value for the address generator synchronous to the switchover signal so that the nozzle rows of a printhead are operated in alternation.

28. An arrangement as claimed in claim 2 wherein the DMA controller comprises at least an executive sequencer, a word counter, a rated value register, an input/output logic, a memory, a comparator and a shift register that are interconnected to one another in order to implement DMA cycles.

29. An arrangement as claimed in claim 28 wherein the input/output logic comprises at least an input for the communicated compression factor, an input for the received DMA start signal and registers for the select signals to be sent, a register for the DMA-busy signal to be sent, a register for the request signal to be sent, an input for the received acknowledge signal, and input for the switchover signal and registers for the address write signal.

30. An arrangement as claimed in claim 2 wherein the printer controller comprises a parameter changer with NAND gates that are interconnected to one another in order to change the compression factor to the value equal to "one" when the high resolution signal has the value equal to "zero" and is switched to the value equal to "one" and in order to change the compression factor to s predetermined, even-numbered value when the high resolution signal has the value equal to "one" and is switched to the value equal to "zero".